REMARKS / ARGUMENTS

Claims 1-31 remain pending in this application.

Priority

Applicants appreciate the Examiner's acknowledgment of the claim for priority and safe receipt of the priority document.

35 U.S.C. §§102 and 103

Claims 1-5 and 7-31 stand rejected under 35 U.S.C. §102(e) as being anticipated by Nishizawa et al (U.S. Patent No. 6,573,567). Claim 6 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Nishizawa et al in view of Ohie (U.S. Patent No. 6,580,164). These rejections are traversed as follows.

The present invention can be distinguished from the cited reference by reference to the drawings, by way of example only, and not by way of limitation. The signal interconnection between pads (11A, 11B) of a control chip (10) and pads (21A, 21B) of a memory chip (20), controlled by control chip (10) is contained in the package. The signal interconnection is achieved via a first bonding wire (16, which is a relatively short wire) connecting pads (11A, 11B) of control chip (10) with the inner lead of the first lead (2c, 2d) and third bonding wire (16, which is a relatively long wire) connecting the inner lead of the first lead (2c, 2d) with pads (21A, 21B) of the

memory chip (20). Therefore, by randomly selecting a single lead from among a plurality of leads of the lead-frame, signal interconnection between the control chip and the memory chip can be achieved without requiring plural kinds of lead-frames and/or a special class of control chip having extra bonding pads. As such, the overall cost of the package can be reduced.

On the other hand, Nishizawa et al, disclose a first chip (34a) and a second chip (34b), which are the non-volatile memory chips for a flash memory, and the controller chip (33), which is provided at a different portion on the substrate from the first chip (34a) and the second chip (34b). The structure of Nishizawa et al is directed to an IC card having a wiring substrate (1) whose structure does not need leads having inner leads and outer leads as in the present invention. This structure is clearly shown in Fig. 5, for example. Therefore the purpose and effect of Nishizawa et al is completely different from the present invention.

The deficiencies in Nishizawa et al are not overcome by resort to Ohie et al. As stated in the previously filed response, Ohie et al, at a minimum, does not disclose a third bonding wire for connecting a third bonding pad on a second semiconductor chip with an inner lead portion of a first lead. Indeed, the Examiner merely relies upon Ohie et al for the showing of a first semiconductor chip being used as a microcomputer while a second semiconductor chip is used as an EEPROM.

In light of the status of the prosecution of this application, Applicants request the Examiner to conduct an interview with the undersigned to expedite prosecution and resolve any remaining issues. In the regard, the Examiner is hereby requested to contact the undersigned by telephone to arrange a suitable time for the interview.

Conclusion

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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